Decoupling Optimization for IC-Package and PCB Systems
Considering High Performance Microprocessor Core and Signal Interface Interactions

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Abstract
The purpose of this paper is to present a modeling and simulation based efficient DECAP optimization process for high performance microprocessor systems consisting of IC-package and PCB, considering the interactions due to mutual coupling of power delivery networks (PDNs) for core and signal interface, corresponding to multiple power boundaries. Effectiveness of the on-die capacitances and package mounted DECAPS on IC-package and PCB for optimizing the input impedance of multiple PDNs is described and illustrated with several simulation results.

1. Introduction
The modern microprocessor systems require multiple power domain or boundaries corresponding to multiple cores and IO interfaces. The IC-packages and printed circuit boards (PCB) with multiple sections of power/ground planes are commonly used for the power delivery networks (PDNs) of such microprocessors based system. The multiple core logic circuits and IO interfaces, switching large dynamic current at fast slew rates through mutually coupled parasitic of package and PCB generate unwanted electrical noise. The interaction of noise generated on multiple power domains creates serious power and signal integrity issues in these microprocessor systems. Therefore, designing PDNs for multiple power boundaries to supply large amount of power at low voltages to different cores and IOs of a microprocessor system is a challenging task.

In general, a high-performance power delivery system consists of printed circuit board (PCB) with voltage regulator modules (VRM), necessary decoupling capacitors (DECAPS), and IC-packages with on-die capacitances for core logic circuits and IO-interfaces [1-2]. The core and IOs circuits operating at low power supply voltages and high frequency with fast switching currents through the power-ground input impedance of the PDNs of the package and PCB induce mid and high frequency power supply noise. The excessive power-ground noise limits the maximum operating frequency of the high-performance microprocessor systems. Similarly, the simultaneous switching noise (SSN) due to switching transitions of several I/Os at the same time causes timing and signal quality related issues in the microprocessor systems. SSN and crosstalk are function of the number of the simultaneously switching I/Os and the loop inductances of the signal-to-power and signal-to-ground, corresponding to high-to-low and low-to-high switching of the IOs. In general, the signal integrity performance of the system consisting of the IO interfaces significantly depends on its power integrity performance.

Decoupling optimization for the PDNs routed through IC-package and PCB of high performance microprocessor systems with cores and signal interfaces are commonly used to eliminate the resonant peaks and reduce the power-to-ground input impedance. Typically, the PDN of a single power domain is considered at a time for DECAP optimization in order to improve its power integrity performance. Similarly, DECAPS for a package and the PCB of a microprocessor system are optimized separately. The parameters of the DECAPS on packages are estimated without considering the on-die capacitances used for different power domains. Also, the package mounted DECAPS are optimized considering the narrowband single-section lumped PDN electrical model, ignoring the high frequency resonant peaks of the input impedance [3]. It is imperative to model and simulate the mutually coupled multiple PDNs of the microprocessor system consisting of the voltage regulator module (VRM), printed circuit board (PCB) and the package together for the accurate optimization of on-die, on-package and on-PCB DECAPS for designing the resonance free power ground input impedance over a sufficiently wide frequency range.

This paper presents an efficient modeling, simulation and analysis methodology for optimizing mutually coupled multiple PDNs of a microprocessor system consisting of a VRM, a multi-layer flip-chip ball-grid array (FCBGA) package and a PCB. The impact of on-die capacitance used for one power domain on the other power domains, for example, the impact of on-die capacitance of a core PDN on the IO-PDN are described in detail. The effect of mutual coupling between the PDNs of multiple power domains is considered for the overall optimization of input impedances of PDNs. The methodology allows fast and accurate frequency domain modeling and simulation of the system consisting of VRM, FCBGA package with multiple power domains and a PCB for DECAP parameter estimations needed to optimize input impedances over a wide frequency range. An efficient computation process for studying the interactions of input impedances of PDNs and the effectiveness of placement of different types of DECAP are discussed to demonstrate the effectiveness of the method.

The multi-layer FCBGA package and PCB can be electrically modeled using a commercially available electromagnetic field solver. The frequency domain characterization based electrical modeling of the PCBs and package using the field solver takes into account the electromagnetic field interactions between different components of the PCBs and the packages. These electrical models are then assembled together for evaluating the power-ground input impedances of PDNs corresponding to multiple power domains. The coupled models of these PDNs are used to evaluate the effectiveness of on-die capacitance of different power domains/boundaries for the core logic circuits and IO circuits. The parameters of the DECAPS needed on the package and PCB corresponding to on-die capacitances can be obtained using these electrical models. The electrical models of the VRM, the FCBGA package PCB, on-die
capacitance and DECAPS can be combined easily for fast and accurate "what-if" analysis. While the analysis methodology described in this study is similar to [4-5], it has the advantage of combining the broadband electrical model of the PCB with the FCBGA package directly inside the electromagnetic field solver with integrated capability of SPICE electrical simulation.

Section 2 of this paper focuses on the electrical modeling of the PDNs of the multiple power domains corresponding to core logic circuits and the high-speed parallel interface. Section 3 mainly focuses on the input impedance simulation and analysis of the PDNs of the FCBGA package individually as well as combined with the PCB and VRM. Section 4 presents the detailed modeling, simulation results of the input impedance of the PDN of a core power domain, considering the effect of connecting the package to the PCB with VRM. The input impedances of the PDNs at different locations, for example (i) on the PCB with or without VRM, DECAPS, and package with or without on-die capacitance and discrete DECAPS and (ii) on the package with or without discrete DECAPS corresponding to different values of the on-die capacitances used for multiple power domains are compared. Transfer impedances are calculated so that the noise coupled between different power boundaries of the microprocessor is also studied.

2. High-speed Digital System Modeling

A simplified high-speed digital system consisting of IC-circuits with multiple power boundaries for supplying power to multiple core circuits and IO interfaces, IC-packages, a multilayer PCB with VRM and a number of decoupling capacitors (DECAPS) mounted on board and the package are shown in Figure 1.

![Figure 1 Block diagram of a high-speed digital System](image1)

The multi-layer PCB and the IC-package are the critical parts of the power delivery networks (PDN) for supplying power to the IC-circuits. The physical characteristics of the multilayer PCB and package of the high-speed digital system shown in Figure 1 are described next.

Multilayer Printed Circuit Board

A printed circuit board with a microprocessor is considered as an example in this paper. The power to the IC-circuits is typically delivered from a VRM connected at the edge connector of the PCB [6]. The power-ground paths from the VRM through the PCB and IC-package to the core and IO circuits of microprocessor at Unit 17 on the top layer of the PCB is the PDN of the interest in this paper for the power integrity performance of the system. The top view and bottom view of the six-layer printed circuit board with dimension of 100 mm by 60 mm are shown in Figure 2 and 3 respectively.

![Figure 2. Top view of the printed circuit board](image2)

![Figure 3. Top view of the printed circuit board](image3)

Figure 4 shows the stackup information of this 6-layer PCB, consisting of with 3 signal layers, one power plane and one ground plane.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (mm)</th>
<th>permittivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 1</td>
<td>0.203</td>
<td>4.5</td>
</tr>
<tr>
<td>Layer 2</td>
<td>0.203</td>
<td>4.5</td>
</tr>
<tr>
<td>Layer 3</td>
<td>0.203</td>
<td>4.5</td>
</tr>
<tr>
<td>Layer 4</td>
<td>0.203</td>
<td>4.5</td>
</tr>
<tr>
<td>Layer 5</td>
<td>0.203</td>
<td>4.5</td>
</tr>
<tr>
<td>Layer 6</td>
<td>0.203</td>
<td>4.5</td>
</tr>
</tbody>
</table>

![Figure 4. Printed Circuit Board Stackup](image4)

Multilayer Flip-chip BGA (FCBGA) package

Next, the 3D view of a multilayer FCBGA-package used as an example for the purpose of DECAP optimization for the power boundaries corresponding to multiple core-PDNs and the IO-PDN of the IC-package and PCB systems is shown in Figure 5(a). The ball-grid array (BGA) or solder-balls, with pitch in the range of 0.8 mm to 1.27 mm, depending on a specific technology covers the entire area on the bottom layer of the package. Figure 5 (b) shows a section of signal nets of the parallel interface to account the effect of simultaneous
switching noise (SSN) in the DECAP optimization process. The solder-bumps (C4s) of the signal, power and ground nets at the bottom layer of the silicon-die are connected to the signal, power and ground solder-balls (C5s) attached to pads on bottom layer of the package through the respective vias, and signal traces on the signal layers of the package, as shown in Figure 5(b). The solder balls (C5s) connect signals, powers, and grounds pins of the silicon-die to the printed circuit board with copper pads in a pattern that matches the solder balls. The signal (S), power (P) and ground (G) nets are distributed for high-speed signal interfaces, such as DDR, with industry recommended S-P-G BGA ratio, typically 6:1:1, to provide the closer return current path to signals and reducing the loop inductance of the IO-PDN. This, in turn significantly improves the power integrity and reduced crosstalk performance of the system [7].

3. PDN Input Impedance Simulation Methodology

The electrical model used in this paper for the decoupling optimization of the PDNs of the IC-package and PCB system, considering core and signal interface interactions due to mutual coupling is shown in Figure 6. The PDNs for multiple cores and IO circuits in a high-speed digital systems consisting of IC package and PCB should be designed such that the input impedance for each of the power domain is resonant-free and of magnitude close to the target impedance over a wide frequency range.

The frequency-domain modeling, simulation and analysis flow process using a commercially available field solver for this purpose is illustrated in Figures 7. Typically, the broadband behavioral model of the PCB, with/without VRM and with/without DECAPS can be generated from the multiport S-parameter model, using a commercially available tool [8]. The behavioral models of the PCB with terminals for signal, power and ground nets can be easily connected to the respective signal, power and ground nets on the board-side of the multilayer FCBGA package file directly imported inside a commercially available electromagnetic field solver.

In general, the multi-terminal electrical models of the PCB and packages can be combined or connected in several ways giving rise to numerous methodology flow for the overall computations of the input impedances of the PDNs corresponding to the DECAP optimization of the IC-package and PCB systems considering Core and IO-interface interactions. One of the methods to compute the power-to-ground input impedances of the PDNs of the IC-package and PCB combined is described in the flow diagram of Figure 7.

Another similar method is based upon first computing the S-parameters for each of the PDNs and signal transmission networks (STNs) on the PCB, without DECAPS. Next, the input impedances of the core-PDNs and the IO-PDN of the PCB without DECAPS can be obtained from these S-parameters by shorting the VRM port directly or by means of the VRM circuit model as shown in Figure 6. A behavioral electrical model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool. Next, in order to study the effect of the on-die capacitances on the PDNs of the PCB plus the package system, the S-parameter or behavioral model of the PDNs and STNs of the PCB can be obtained using a commercially available tool.
4. Simulation and Analysis Results

The modeling, simulation and analysis methodology described in sections 2 and 3 has been used to evaluate the input impedance characteristics of PDNs of core and IO circuits of a high-speed digital system. The input impedance characteristics are obtained by considering a number of configurations of the PCB, package and PCB plus package systems. These configurations differ in terms of the number, types and locations of DECAPS placed on the package and on the PCB to optimize the input impedances of coupled PDNs.

Figure 7. Frequency domain modeling and simulation flow for DECAP optimization of IC-package systems

The goal is to realize each PDN input impedance as resonant-free and of magnitude close to a specified target impedance over a wide frequency range. Typically, the frequency range for input impedance optimization is from DC to 4 or 5 times the frequency of operation of core logic circuits for the core-PDNs and DC to 4 or 5 times the frequency of operation of the high-speed signal interface for the IO-PDN.

The input impedances can be minimized in the low frequency region by connecting external DECAPS of appropriate values across the VRM terminals on the PCB. The VRM circuit modeling and the effects of connecting DECAPS across VRM terminals on the PCB is discussed next.

Voltage Regulator Module (VRM)

A voltage regulator module (VRM) is commonly used in a high-speed digital system for the purpose of feeding power to core and IO logic circuits. These VRM modules generally use buck, boost or buck-boost DC-to-DC converter circuit topology with closed-loop feedback circuits for regulating the voltage at a load point. A simple behavioral lumped circuit model of a VRM, as shown in Figure 6, is sufficient in the initial design phase of PDNs of the high-speed digital systems.

The lumped circuit model of the VRM consists of an ideal voltage source and four passive elements. The values of these passive elements can be found from the output impedance characteristic of the VRM, as shown in Figure 8. These characteristics are typically available from the DC-to-DC converter manufacturer. The value of the inductance L and capacitance C can be obtained from a point, such as A, in the inductive portion and a point in the capacitive portion, such as B, of the impedance characteristics of the VRM. Assuming the value of the quality factor Q for a parallel resonant circuit, typically as 0.707, the value of the resistance R can be found from $Q = \frac{R}{f_0 L}$, where $f_0$ is the parallel-resonant frequency (at point C) of the VRM. The constant output impedance of the VRM in the upper frequency range can be assumed as the impedance of the parallel combination of R and the ESR of the capacitor, R. Therefore, using the computed value of R, value of R can be obtained from a point, such as point D, in the flat portion of the VRM impedance magnitude plot.

It is important to note that the output impedance magnitude of the VRM, as shown in Figure 8, can be reduced by placing external decoupling capacitors across the VRM terminals on the PCB. The decoupling capacitor is represented as the series connected capacitance C, with its ESR, R, and ESL L as in Figure 6.
elements found from the output impedance characteristics of the VRM, the effect of the external DECAPS being connected at the terminals of the VRM on the PCB is shown in Figure 9.

Figure 9. Output impedance magnitude of a VRM

The input impedance looking into the board at Unit 17 can be obtained by shorting the port at the edge connector location. The input impedance of the core-PDN, with and without DECAPS on the PCB, as shown in Figure 10, is obtained over a frequency range of dc to 6 GHz. Note that the input impedance for both, with and without DECAPS on the PCB, becomes inductive at 100 kHz.

Figure 10. Power-ground input impedance of the PCB

The values of the DECAPS in order to lower the input impedance over a wide frequency range are selected to reduce the resonant peaks of the input impedance of the core-PDN. Some of the DECAPS are placed at the specified locations on top layer of the PCB, as close as possible to Unit 17 for the microprocessor location. Additional DECAPS are placed on the bottom layer of the PCB in order to reduce the power ground noise generated on the PCB. Note that the input impedance magnitude is reduced by using eight 0.022 μF DECAPS on the top layer of the board, twenty 0.01 μF and eight 1.0 μF DECAPS on the bottom layer of the board.

Figure 11 shows the input impedances of the PCB’s core-PDN without DECAPS, looking from the Unit 17, with edge connector being terminated using (i) short, (ii) \( R = 1 \text{ mΩ} \), (iii) \( R = 50 \text{ mΩ} \), (iv) \( R = 50 \text{ mΩ} \) in parallel to \( L = 0.5 \mu \text{H} \), and (v) VRM lumped circuit model: parallel combination of \( R_r = 50 \text{ mΩ} \) and \( L_r = 0.5 \mu \text{H} \) in parallel with the series combination of \( R_d = 10 \text{ mΩ} \) and \( C_d = 200 \mu \text{F} \).

Figure 11. Power-ground input impedance of the PCB without DECAPS, using different termination schemes

The input impedances of the core-PDN of the PCB, without DECAPS and with 36 DECAPS, terminated at the VRM location using its lumped circuit model with different number of external DECAPS across are shown in Figure 12.

Figure 12. Power-ground input impedance of the PCB without DECAPS, using VRM termination schemes

Note that the input impedance of the core-PDN of the PCB with 36 DECAPS is reduced in the low frequency range due to its edge being terminated by connecting different number of external DECAPS across the VRM terminals.

**PDN Input Impedances of the FCBGA-package**

The self-input impedances of the PDNs of the multiple core power domains and the PDN for the IOs (IO-PDN) of
the FCBGA-package, with different number of IOs switching simultaneously are shown in Figure 13.

Figure 13. Self-input impedances of the PDNs of the package

Note that the first peak of the self-input impedance of the IO-PDN decreases with increasing number of IOs switching simultaneously.

Typically, on-die capacitances are connected between the power and ground terminals to realize the resonant free-input impedance of low magnitude, in order to improve the power integrity performance of the IC-packaging systems. The effect of on-die capacitance of different values on the self-input impedances of IO-PDN with different number of IOs switching simultaneously is shown Figure 14.

Figure 14 illustrates that the increasing value of the on-die capacitance shifts the resonant peak of the IO-PDN input impedance to the lower frequency range and the impedance magnitude is significantly reduced over a wide frequency range after the resonant peak. The amplitude of this shifted resonant peak can be further reduced by using the package mounted DECAPS with optimum number of DECAPS with capacitance, ESL and ESR values selected appropriately.

The IO-PDN input impedances with nine on-package DECAPs, in addition to the on-die capacitance of a given value is shown in Figure 15. The capacitance value of a package mounted DECAP is computed using ESL = 150 pF and the series-resonant frequency equal to or greater than the peak input impedance frequency corresponding to on-die capacitance of values 1 nF, 5 nF and 10 nF respectively.

Figure 15. Self-input impedance of the IO-PDN with different values of on-die and on-package DECAPS

The peak amplitude of the input impedance is reduced by using nine DECAPS on the FCBGA-package. Also, the resonant peak of the input impedance reduces more with the increasing value of the ESR.

The transfer input impedance between the IO-PDN and the core0-PDN for different values of the on-die capacitance for the IO-PDN with 59 IOs switching simultaneously is shown in Figure 16. Note that the transfer impedance, which implies the amount of noise coupling from IP-PDN to Core0 PDN is reduced with increasing value of on-die capacitance.

Figure 17 shows the transfer input impedance between the IO-PDN and the core0-PDN for on-die capacitance of the same value used either for the core-PDN or for the IO-PDN with 59 IOs switching simultaneously. It is important to note that the transfer input impedance between the IO-PDN and the core-PDN is reduced more with on-die capacitance of a given value placed across the core-PDN as compared to the same value of on-die capacitance connected across the IO-PDN.
Figure 17. Transfer-input impedances for same value of on-die capacitance either across core-PDN or IO-PDN

**PDN Input Impedances of the PCB and FCBGA-package**

The self-input impedances of the PCB without DECAPS, FCBGA-package and FCBGA-package connected to PCB without DECAPS are shown in Figure 18. Figure 18 illustrates that the input impedance of the PDN of the FCBGA-package dominates the input impedance of the PDN of the PCB connected with the FCBGA-package.

Next, the input impedances of the FCBGA-package connected to the PCB without DECAPS are obtained by (i) shorting the edge connector and (ii) by terminating the edge connector using the lumped model of the VRM. Also the input impedances of the PCB with 36 DECAPS of different values (eight 0.022 µF, on the top layer, twenty 0.01 µF and eight 1.0 µF on the bottom layer), mounted with FCBGA-package including the on-die capacitance of 10 nF, 20 nF and 40 nF are obtained by terminating the edge connector on the PCB with the lumped connector on the PCB with the lumped circuit model of the VRM connected with four DECAPS (as shown in Figure 8) across its terminal on the PCB. These input impedances of the IO-PDN are shown in Figure 18.

Figure 18. Power-ground input impedance of the PCB, package and package plus PCB without DECAPS

Figure 19 illustrates that the overall input impedances of the IO-PDN of the PCB with 36 DECAPS, mounted with FCBGA package including the on-die capacitance of a specific value across the IO-PDN of the package, and the VRM with 4 DECAPS across its terminal on the PCB are reduced as compared to the input impedance of the PCB without DECAPS mounted with the VRM.

**5. Conclusions**

Based on the network representation of the PCB, VRM and DECAPS connected to the FCBGA package in a field solver, an efficient simulation and analysis methodology for decap optimization for multiple power domains, considering core and signal interface interactions is described. The methodology provides the computational process for the optimization of input impedances of the coupled multiple PDNs. Simulation results for different configurations of the PCB and package with on-die capacitances, discrete DECAPS and VRM are discussed in detail. It is recommended that the decoupling optimization for the multiple power boundaries of IC-package and PCB system should be performed considering the core and signal interface interactions with maximum number of IOs switching simultaneously.

A comparative study of effectiveness of the on-die capacitance in optimizing the package mounted discrete DECAPS for realizing the resonant free input impedance of target magnitude required for reducing the Core-PDN and IO-PDN noise is described and illustrated with several simulation results.

**References**


[3] Om P. Mandhana, “Package Electrical Characterization Dependent Power and Signal Integrity Simulation-


